



JFW

Docket No.: 057454-0972

PATENT**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

In re Application of : Customer Number: 20277
Hideto HIDAKA : Confirmation Number: 2444
Application No.: 10/663,674 : Group Art Unit: 2824
Filed: September 17, 2003 : Examiner: PHUNG, ANH

For: THIN FILM MAGNETIC MEMORY DEVICE HAVING DATA READ CURRENT TUNING FUNCTION

INFORMATION DISCLOSURE STATEMENT

Mail Stop IDS
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

In accordance with the provisions of 37 C.F.R. 1.56, 1.97 and 1.98, the attention of the Patent and Trademark Office is hereby directed to the references listed on the attached form PTO-1449. It is respectfully requested that the references be expressly considered during the prosecution of this application, and that the references be made of record therein and appear among the "References Cited" on any patent to issue therefrom.

This Information Disclosure Statement is being filed within three months of the U.S. filing date OR before the mailing date of a first Office Action on the merits. No certification or fee is required.

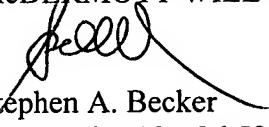
Each non-English language reference was first cited in a corresponding foreign application search report or office action and its relevance discussed therein. A copy of the

foreign search report or office action, together with an English language version thereof, is attached for the Examiner's information.

Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

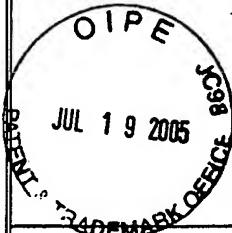
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**Please recognize our Customer No. 20277
as our correspondence address.**

INFORMATION DISCLOSURE CITATION IN AN APPLICATION  (PTO-1449)				ATTY. DOCKET NO. 057454-0972	SERIAL NO. 10/663,674	
				APPLICANT Hideto HIDAKA		
FILING DATE September 17, 2003				GROUP 2824		
U.S. PATENT DOCUMENTS						
EXAMINER'S INITIALS	CITE NO.	Document Number Number-Kind Code ₂ (<i>if known</i>)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	
	A1	US 2003/0002333	01/02/2003	Hidaka		
	B1	US 6,185,130	02/06/2001	Hollmer et al.		
	B2	US 6,856,539	02/15/2005	Hidaka		
	US					
FOREIGN PATENT DOCUMENTS						
EXAMINER'S INITIALS	CITE NO.	Foreign Patent Document Country Code ₂ -Number 4-Kind Codes (<i>if known</i>)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines Where Relevant Figures Appear	Translation Yes No
	A2	EP 1 225 591	07/24/2002	Kabushiki Kaisha Toshiba		
	A1	DE 101 30 829 w/English abstract	07/18/2002	Mitsubishi Electric Corp.		
	A1	DE 102 28 578 w/English abstract	01/16/2003	Mitsubishi Electric Corp.		
OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)						
EXAMINER'S INITIALS	CITE NO.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.				
		SCHEUERLEIN, R.; GALLAGHER, W.; PARKIN, S.; LEE, A.; RAY, S.; ROBERTAZZI, R.; REOHR, W.: "A 10 ns read and write non-volatile memory array using a magnetic tunnel junction and FET switch in each cell" IEEE International Solid-State Circuits Conference, 7-9 Feb. 2000, 128-129				
		NAJI, P.K.; DURLAM, M.; TEHRANI, S.; CALDER, J.; DEHERRERA, M.F.: "A 256 kb 3.0 V 1T1MTJ nonvolatile magnetoresistive RAM" IEEE International Solid-State Circuits Conference, 5-7 Feb. 2001, 122-123, 438				
		YAMADA, K.; SAKAI, N.; ISHIZUKA, Y.; MAMENO, K.: "A novel sensing scheme for an MRAM with 5% MR ratio" Symposium on VLSI Circuits, 14-16 June 2001 123-124				
		TEHRANI, S.; ENGEL, B.; SLAUGHTER, J.M.; CHEN, E.; DEHERRERA, M.; BURLAM, M.; NAJI, P.; WHIG, R.; JANESKY, J.; CALDER, J.: "Recent developments in magnetic tunnel junction MRAM" IEEE Transactions on Magnetics, Vol. 36, No. 5, Sept. 2000, 2752-2757				
		SCHEUERLEIN, R.E.: "Magnetoresistive IC memory limitations and architecture implications" 7th Biennial IEEE Nonvolatile Memory Technology Conference, 22-24 June 1998, 47-50				
		FREITAS, P.P.; CARDOSO, S.; SOUSA, R.; WANJUN KU; FERREIRA, R.; CHU, V.; CONDE, J.P.: "Spin dependent tunnel junctions for memory and read-head applications" IEEE Transactions on Magnetics, Vol. 36, No. 5, Sept. 2000, 2796-2801				
EXAMINER			DATE CONSIDERED			

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered.
 Include copy of this form with next communication to applicant.

1 Applicant's unique citation designation number (optional). 2 Applicant is to place a check mark here if English language Translation is attached.